

TSMC00-079

thereby forming a via hole;

depositing a layer of copper to a thickness sufficient to fill the via hole and to overfill the wiring trench; and

*B3 end*  
by means of chemical mechanical polishing, removing copper until said wiring

5 trench is just filled and there is no copper on any exposed surface outside the trench, thereby forming said damascene structure and whereby said damascene structure is free of cracking and peeling.

#### REMARKS

Examiner Vinh is thanked for his ongoing examination of our application.

Reconsideration of the rejection of all claims is respectfully requested. We wish to comment on his remarks as follows:

Reconsideration is requested of all rejections based on 35 U.S.C. 112

The phrase "with no intervening steps" has been removed from all claims, as required by Examiner.

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The word "predetermined" has been removed from all claims, as required by Examiner.

In conclusion, we again thank Examiner Vinh for his careful reading of our application. Reconsideration and withdrawal of the rejection is respectfully requested.

Allowance of all Claims is requested. It is also requested that should Examiner Vinh not find that the Claims are now Allowable, he should please call the undersigned Attorney at (845)-452-5863 to overcome any problems preventing Allowance.

Respectfully submitted

A handwritten signature in black ink, appearing to read "SBA".

Stephen B. Ackerman #37761

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**In the claims:**

**RECEIVED**

JUN 12 2002

**Please amend the following claims:**

**TC 1700**

1.(twice amended) A process for forming a layer of low dielectric constant material having a [predetermined] thickness, comprising:

depositing a first layer of low dielectric constant material by means of plasma enhanced vapor deposition, at a first power level;

5 then[, with no intervening steps,] depositing a second layer of the low dielectric constant material by means of plasma enhanced vapor deposition, at a second power level that is higher than said first power level; and

repeating the preceding two steps until said [the predetermined] thickness is reached.

10 9.(twice amended) A process for depositing a layer of black diamond on a silicon wafer to a [predetermined] thickness, comprising:

through chemical vapor deposition, from a first gaseous mixture of methyl silane and nitrous oxide, enhanced by a helium plasma at a power level that is less than about 70 watts, depositing a low power layer of black diamond for about 10 seconds, thereby

forming a layer having a thickness between about 700 and 1,000 Angstroms;

then[, with no intervening steps,] through chemical vapor deposition, from a second gaseous mixture of methyl silane, nitrous oxide, and oxygen, enhanced by a helium plasma at a power level of between about 70 and 200 watts, depositing a high power layer 5 of black diamond for about 10 seconds, thereby forming a layer having a thickness between about 700 and 1,000 Angstroms; and

repeating the preceding two steps until said [predetermined] thickness is reached.

14.(twice amended) A process for forming a dual damascene structure on a silicon wafer, comprising:

10 through chemical vapor deposition, from a first gaseous mixture of methyl silane and nitrous oxide, enhanced by a helium plasma at a power level that is less than about 70 watts, depositing a low power layer of black diamond for about 10 seconds, thereby forming a layer having a thickness between about 700 and 1,000 Angstroms;

then[, with no intervening steps,] through chemical vapor deposition, from a second

15 gaseous mixture of methyl silane, nitrous oxide, and oxygen, enhanced by a helium plasma at a power level of between about 70 and 200 watts, depositing a high power layer of black diamond for about 10 seconds, thereby forming a layer having a thickness between about 700 and 1,000 Angstroms;

repeating the preceding two steps until a completed black diamond layer has been

20 formed;

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patterning and etching said completed black diamond layer in order to form a wiring trench;

patterning and etching said wiring trench down to the level of the silicon wafer, thereby forming a via hole;

5       depositing a layer of copper to a thickness sufficient to fill the via hole and to overfill the wiring trench; and

by means of chemical mechanical polishing, removing copper until said wiring trench is just filled and there is no copper on any exposed surface outside the trench, thereby forming said damascene structure and whereby said damascene structure is free  
10      of cracking and peeling.